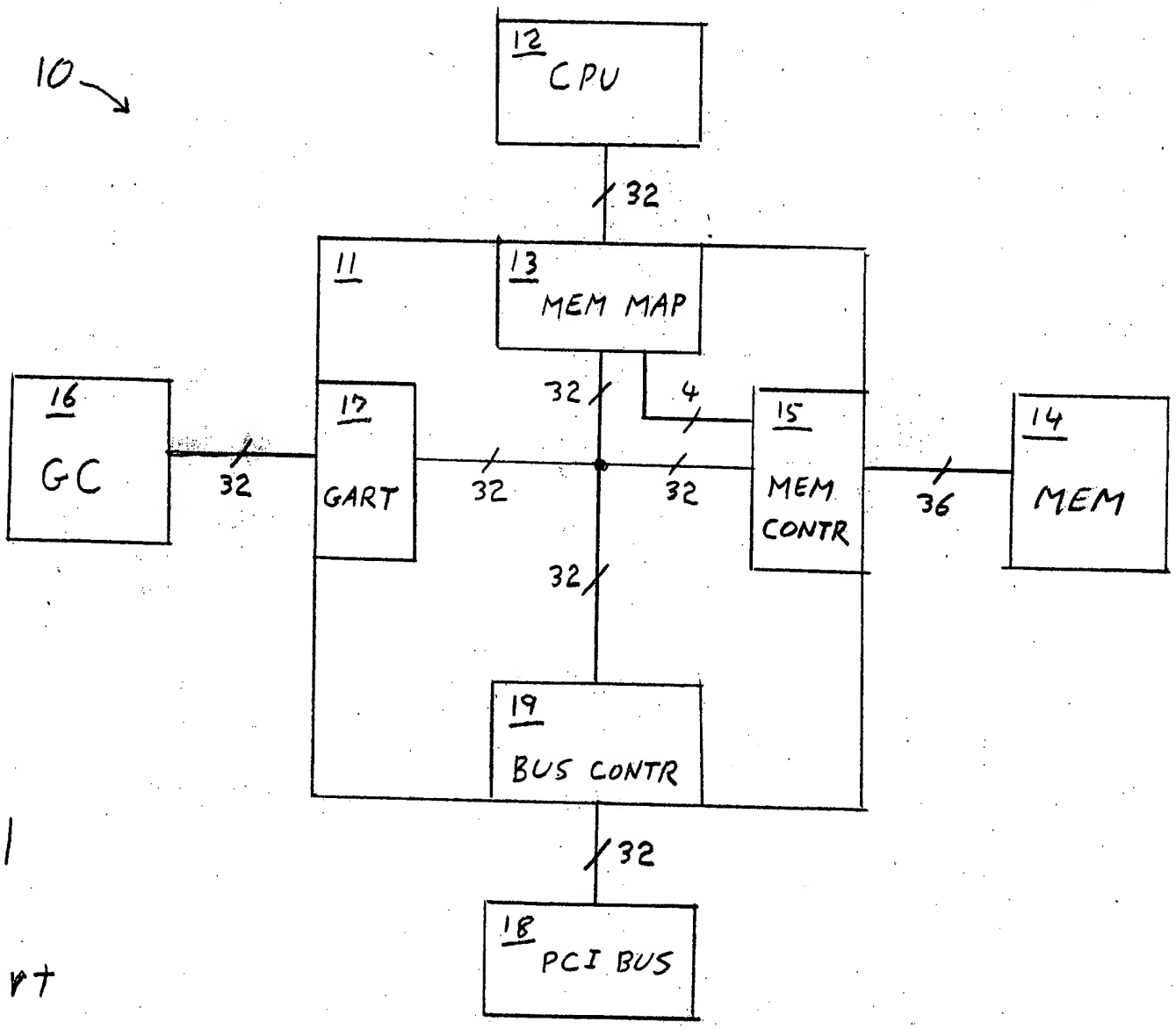

Fig. 1

Prior Art

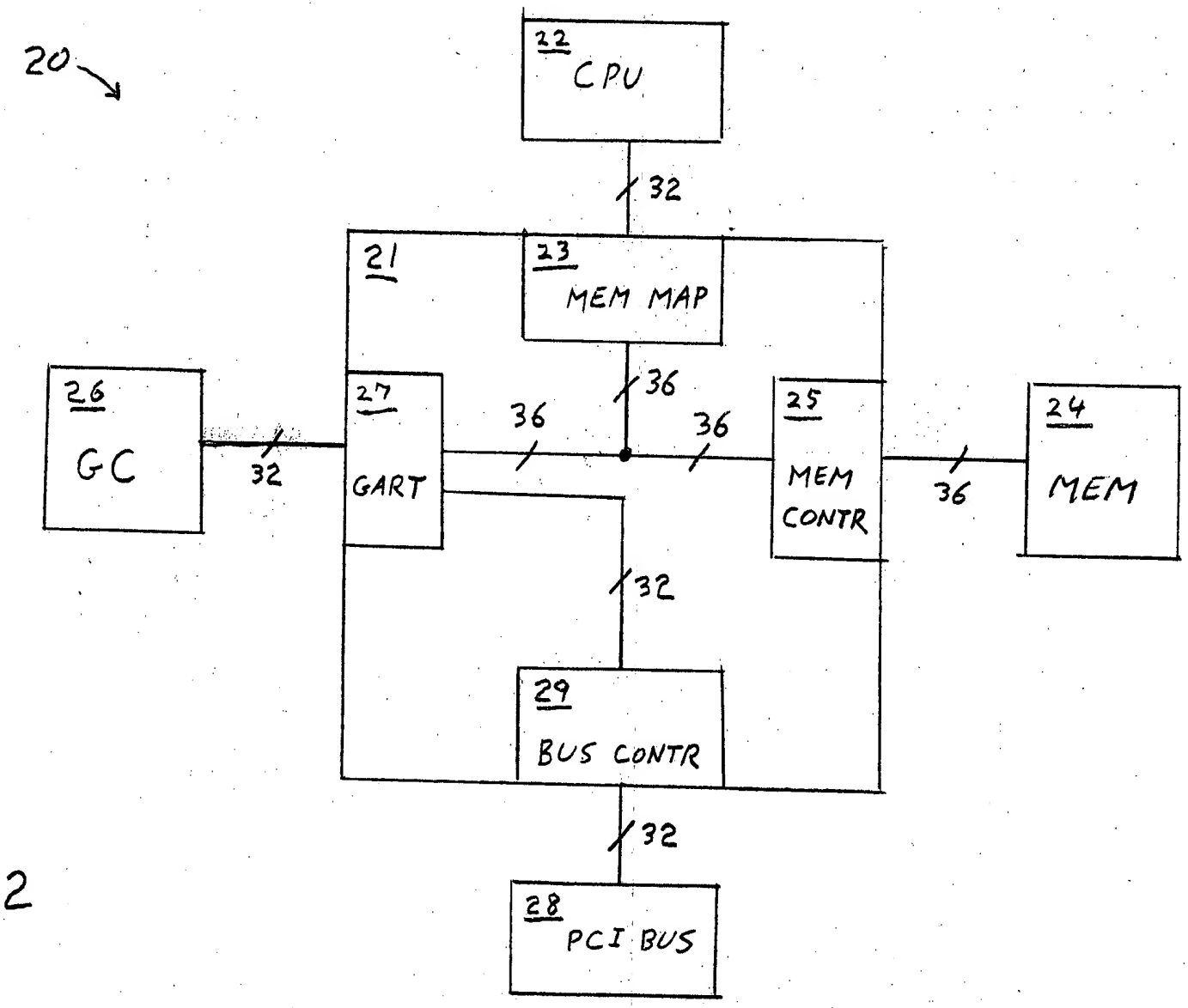
20
22
CPU
32
21
23
MEM MAP
36
36
36
26
GC
32
27
GART
25
MEM
CONTR
36
24
MEM
32
29
BUS CONTR
32
28
PCI BUS

Fig. 2

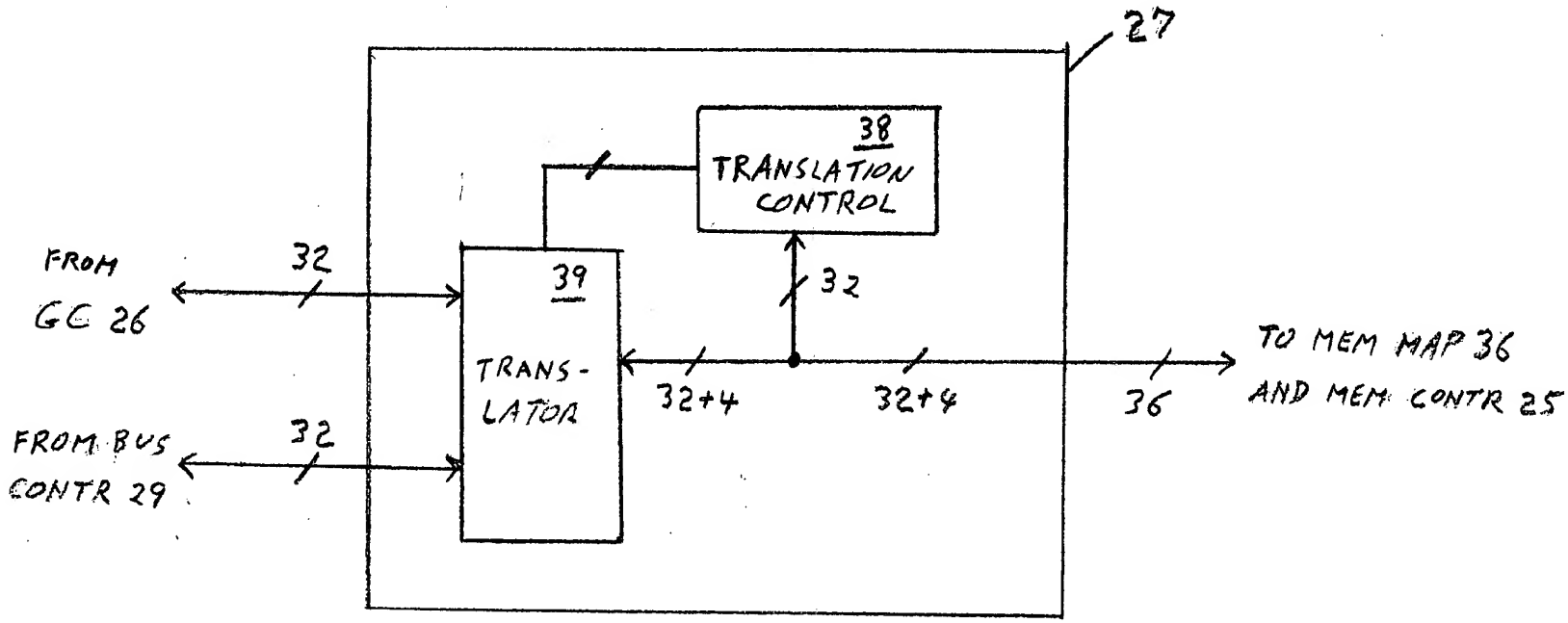
27
38
TRANSLATION CONTROL
FROM GC 26
32
39
32
TRANS-LATOR
TO MEM MAP 36 AND MEM CONTR 25
32+4
32+4
36
FROM BUS CONTR 29
32

Fig. 3

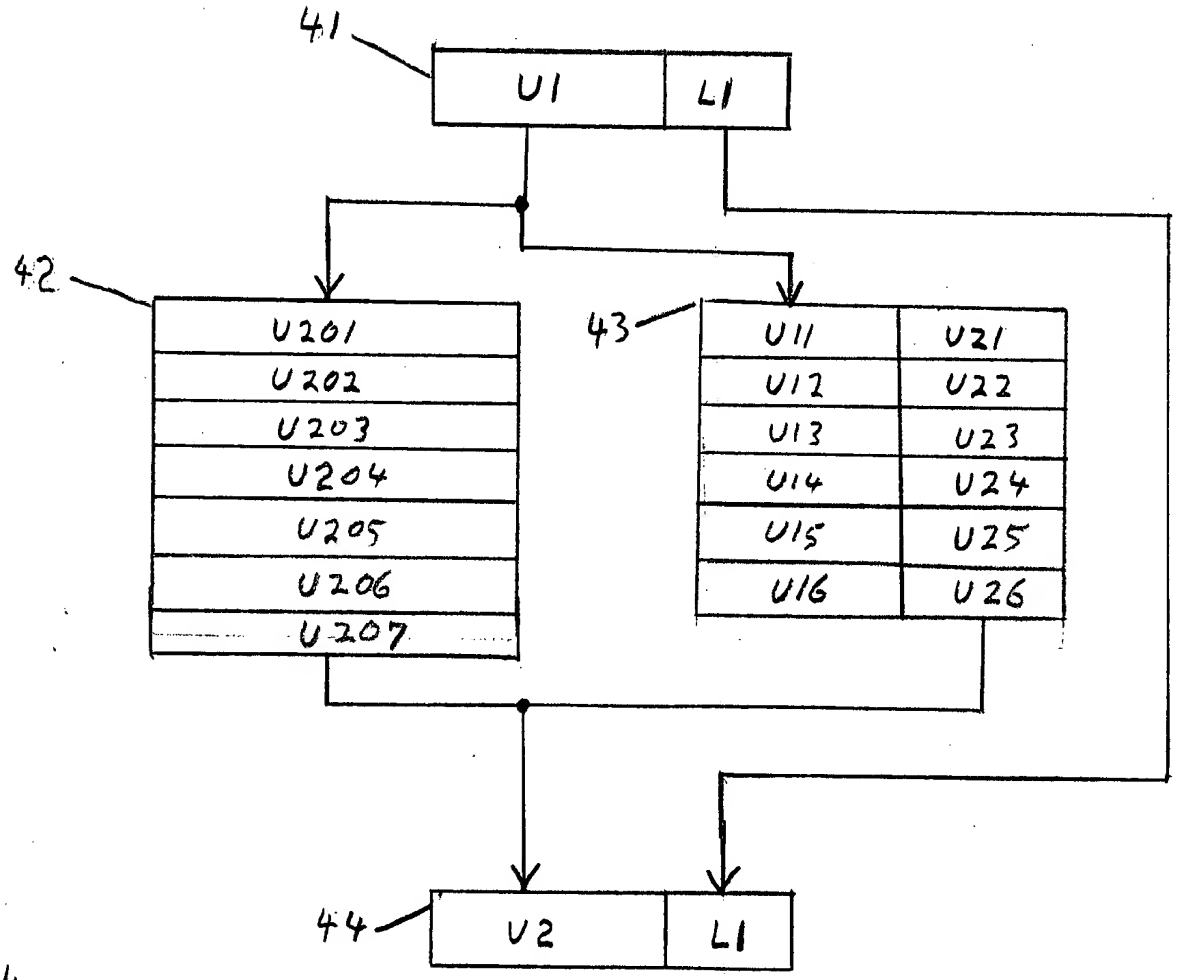
41
U1
L1
42
U201
U202
U203
U204
U205
U206
U207
43
U11
U21
U12
U22
U13
U23
U14
U24
U15
U25
U16
U26
44
U2
L1

Fig. 4